A COMPLETE SYSTEM-ON-CHIP DESIGN ENVIRONMENT

GRLIB IP Library

The GRLIB IP Library is a complete System-on-Chip (SoC) design environment which includes a collection of reusable VHDL IP cores targeting FPGA and ASIC designs. The library uses a consistent method for simulation and synthesis, making it easy to use with different third-party EDA tools.

GRLIB is designed to be used in digital system designs independently of the target technology vendor. It supports various FPGA technologies (e.g., AMD/Xilinx, Intel/Altera, Lattice, Microchip, and NanoXplore). GRLIB IPs utilize a technology abstraction layer, enabling easy portability between technologies as well as a straightforward way for end-users to add support for additional technologies. All microprocessor IPs and most peripherals are proven in both FPGA and ASIC implementations. GRLIB offers an efficient and cost-effective solution for digital system design, reducing development time and expenses.

IP Cores

- Processors: LEON SPARC processors, NOEL-V RISC-V processor, L2 cache, Timers, Interrupt controllers
- Memory controllers: DDR2/DDR3 SDRAM, 32-bit PC133 SDRAM, SRAM, QSPI, NANDflash, parallel PROM
- Interfaces: SpaceWire endpoint and router, SpaceFibre and WizardLink controller, 32-bit PCI bridge, CCSDS/ECSS Data Handling, 10/100/1000 Mbit Ethernet MAC, USB 2.0 host and device controllers, SelectMap FPGA Supervisor, CAN FD, MIL-STD-1553B, SPI, I2C, UART
- SoC infrastructure: AHB and APB controllers, AHB to AHB bridge, AHB to AXI bridge

Template Designs

To allow users to quickly get started with their development, GRLIB contains template designs for common commercial FPGA evaluation boards. Template designs for SoC development contain commonly used IP cores such as processors, memory controllers and communication interfaces tailored for specific development boards and with targeted constraints. They provide a reliable starting point for customization and optimization, enabling designers to concentrate on the unique aspects of their SoC design.

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Debugging

The GRMON3 hardware debugger enables developers to efficiently diagnose and resolve issues. With drivers that simplify the control of processors and peripherals, GRMON3 provides a powerful tool for troubleshooting complex systems. The debugger has the ability to connect to the SoC through various types of communication interfaces for monitoring and testing purposes. This allows developers to debug their systems at all stages of the design process, from the early stages of hardware bring-up to the final stages of software development.

Licensing

The GRLIB IP Library is available in both open-source and commercial versions. The open-source version is distributed under the GNU GPLv2 license, making it ideal for academic purposes, evaluation, and prototyping. However, the GPLv2 license poses restrictions on commercial products, so GRLIB presents a commercial licensing option for those who require proprietary designs. The commercial distributions provide access to additional IPs and target technologies not included in the open-source version. The GRLIB IP Core User's Manual provides a complete list of all IP cores, along with information about which GRLIB distribution(s) includes each IP core.

Support

The GRLIB community is a discussion platform that can be used by open-source users of the library to seek help, share information, discuss, and collaborate.

https://grlib.community

GRLIB commercial users can benefit from an optional support agreement that provides them with direct communication with the development team.